

JOSEPH W. PRICE
ALBIN H. GESS
MICHAEL J. MOFFATT
GORDON E. GRAY III
BRADLEY D. BLANCHE
J. RONALD RICHEBOURG

OF COUNSEL
JAMES F. KIRK

PRICE AND GESS

ATTORNEYS AT LAW

2100 S.E. MAIN STREET, SUITE 250

IRVINE, CALIFORNIA 92614-6238

A PROFESSIONAL CORPORATION
TELEPHONE: (949) 261-8433
FACSIMILE: (949) 261-9072
FACSIMILE: (949) 261-1726

e-mail: pg@pgpatentlaw.com

SPECIFICATION, CLAIMS AND ABSTRACT

Inventor(s): Masaaki Nishijima
Title: RF PASSIVE CIRCUIT AND RF AMPLIFIER WITH VIA-HOLES
Attorney's
Docket No.: NAK1-BP73

EXPRESS MAIL LABEL NO. EL873069933US
DATE OF DEPOSIT: August 13, 2001

TITLE OF INVENTION

RF PASSIVE CIRCUIT AND RF AMPLIFIER WITH VIA-HOLES

5 BACKGROUND OF THE INVENTION

(1) Field of the Invention

This invention relates to a technology for making smaller and lighter RF passive circuits and RF amplifiers equipped with via-holes.

10

(2) Prior Art

Recently, various types of mobile communication tools, such as portable phones or portable information terminals have been commercialized all over the world. As portable phones, cellular phones for bands of 900 MHz and 1.5 GHz, and Personal Handyphone System (PHS) for a band of 1.9 GHz are two examples that are commercialized in Japanese market. Other examples include world-famous GSM, and CDMA among the technologies adopted in PCS (Personal Communications Services) in the U.S.A.

15
20

As a third-generation mode following the analogue mode and the digital mode, IMT2000 is planned to be commercialized in the future.

In developing mobile communication terminals

especially portable terminals, it is an inevitable trend to seek smaller and lighter terminals. Accordingly, it is important to achieve a technology for making smaller and lighter components for these terminals.

5 As a trend, it is desired to make high frequency components of the portable terminals as a monolithic microwave IC (MMIC). The MMIC, in which active elements, their matching circuits, and bias circuits are integrated on the same substrate, is more advantageous in making
10 smaller products than a Hybrid IC which is structured to have circuits and bias electricity-feeding circuits as outside-chips.

Even using the MMIC, it is required to ground circuit elements. Conventional grounding methods include a method
15 of wire-bonding from the surface of semiconductor substrates, and a via-hole method. It is more effective to use the via-hole method in achieving high-quality and low cost for packaging, which makes the via-hole method more frequently adopted in the MMIC.

20 The following is a description of an example of a conventional type of RF passive circuit and RF amplifier equipped with via-holes with reference to Figs. 8A - 8D.

Fig. 8A is a schematic circuit diagram of a conventional RF amplifier which includes RF passive

circuits equipped with via-holes, and Fig. 8B and 8C are pattern diagrams of conventional RF passive circuits both equipped with a via-hole.

As Fig. 8A shows, a source-ground type of RF amplifier
5 is constructed by connecting: a gate bias resistance 805
and an input matching circuit 806 to a gate terminal 802;
a drain voltage feeding circuit 807 and an output matching
circuit 808 to a drain terminal 803; and a source terminal
804 to a ground terminal 809, in the field effective
10 transistor (FET) 801. An input terminal 810 and an output
terminal 811 are both 50Ω impedance, and the input matching
circuit 806 and the output matching circuit 808 are
adjusted to 50Ω . Further, each of an input DC cut capacitor
812 and an output DC cut capacitor 813 is inserted to the
15 input side and the output side respectively.

The input matching circuit 806 consists of an input
matching parallel inductor 814, an input matching parallel
capacitor 815, and an input matching serial inductor 816.
The input matching parallel capacitor 815 is grounded by
20 an input matching circuit via-hole 821.

The output matching circuit 808 consists of an output
matching serial inductor 817, and an output matching
parallel capacitor 818. The output matching parallel
capacitor 818 is grounded by an output matching circuit

via-hole 822.

The drain voltage feeding circuit 807 consists of a choke inductor 819 and a bypass capacitor 820. The bypass capacitor 820 is grounded by a drain voltage feeding circuit via-hole 823.

Figs. 8B and 8C are both pattern diagrams of an RF passive circuit with a via-hole; each of them shows the input matching circuit 806 and the drain voltage feeding circuit 807 respectively. Fig. 8D shows a cross-sectional view taken along line (A-A') of Fig. 8B. The following is a description of a common part between the input matching circuit 806 and the drain voltage feeding circuit 807, taking an example of the input matching circuit 806.

Constituting elements of the aforementioned input matching circuit 806 is made, as a semiconductor substrate, on a surface of a GaAs substrate 824. Both of the input matching parallel inductor 814 and the input matching serial inductor 816 are made in a spiral-electrode-pattern, and the input matching parallel capacitor 815 is made in an MIM(Metal-Insulator-Metal) capacitor pattern.

As Fig. 8D shows, the spiral-electrode-pattern is made on the GaAs substrate 824 which is covered by an insulator film 834 such as silicon oxide. Specifically, the spiral-electrode-pattern is a structure where a lower

wiring metal layer 831 which is made by gold/titanium vacuum evaporation is connected to an upper wiring metal layer 830 made by gold-plating by means of a contact hole 833, with a between-layer insulator film 832 in between.

5 On the other hand, the MIM capacitor is a structure where an upper wiring metal 829 is formed on a dielectric layer 828 under which is an electrode extended from the lower wiring metal layer 831; the upper wiring metal 829 is made by gold/titanium vacuum evaporation and the
10 dielectric layer 828 is titanium oxide strontium (SrTiO₃:STO) with a permittivity of 100 or more. The end of the electrode extended from the upper wiring metal 829 is connected to a ground metal layer 826 which is situated on the via-hole, as Figs. 8B and 8C show.

15 The input matching circuit via-hole 821 can be formed by etching from the main surface of the GaAs substrate 824 where circuit elements were made (a surface via-hole). Or, it could also be formed by etching from the other main surface (a backside via-hole). Inside the via-hole 821,
20 an electric conducting film is conducted to a backside ground metal 829. This electric conducting film is electrically connected to the upper wiring metal 829 of the MIM capacitor through the ground metal layer 826.

Further, as depicted in Fig. 8C, constituting

elements of the drain voltage feeding circuit 807 are formed, as a semiconductor substrate, on the surface of the GaAs substrate 824. As for the choke inductor 819, a spiral-electrode-pattern is used, and as for the drain
5 voltage feeding circuit via-hole 823, either a surface via-hole or a backside via-hole is used for forming.

Note that a feeding terminal 825 is structured by extending a drain voltage terminal 836 from the lower wiring metal layer 831 through an extending wire 835.

10 Thus structured as above, the following constituting elements of the RF passive circuit are formed on and through the GaAs substrate: the spiral inductor, the MIM capacitor, and the via-hole. Moreover, as Fig. 8C shows, the above three elements are positioned at a different location
15 two-dimensionally, and are connected to each other by wiring. The elements constitute the RF amplifier with a help of the input matching circuit 808 and the drain voltage feeding circuit 807.

20 As seen above, the conventional type of RF amplifiers and RF passive circuits cannot be made smaller in size, due to the two-dimensional positioning of the constituting elements of the drain voltage feeding circuit 807, which inherently take much space.

SUMMARY OF THE INVENTION

Based on the stated problem, the object of the present invention is to realize smaller RF passive circuits and RF amplifiers equipped with via-holes.

5 To achieve the above object, the present invention is characterized by a structure of being equipped with a spiral inductor formed on a main surface of a semiconductor substrate, and a via-hole made from the main surface and through the semiconductor substrate. The via-hole is made
10 at the position adjacent to the spiral inductor, with a dielectric layer and a wiring metal layer formed on a metal film of the via-hole so as to hold a capacity element between the metal film and the wiring metal layer, and the spiral inductor extends at one end to be electrically
15 connected with the wiring metal layer.

The above structure enables to incorporate a capacitor in a via-hole, thereby enabling a three-dimensional location of the following three elements on one semiconductor substrate; a spiral inductor, a
20 capacitor, and a via-hole. Thus reduced occupancy will produce an effect of enabling a smaller RF passive circuit and an RF amplifier made of the RF passive circuits as main components.

Furthermore, the RF amplifier of the present

invention is characterized by a structure of utilizing the RF passive circuit equipped with the via-hole as a matching circuit, or as an RF choke in a bias feeding circuit.

Furthermore, an RF passive circuit of the present invention is equipped with a spiral inductor formed on a main surface of a semiconductor substrate and a via-hole that is made from the main surface and goes through the semiconductor substrate. The via-hole is placed adjacent to the spiral inductor, and on a metal film of the via-hole, a first dielectric layer, a first wiring metal layer, a second dielectric layer, and a second wiring metal layer are formed in this order, so as to form a first capacity element between the metal film of the via-hole and the first wiring metal layer, and a second capacity element between the first wiring metal layer and the second wiring metal layer. The present invention is further structured to have the metal film and the second wiring metal layer electrically connected so as to hold a static capacity determined by a sum of the first capacity element and the second capacity element. The present invention is further characterized by a spiral inductor extending at one end to be electrically connected to the first wiring metal layer.

This structure will help to make a smaller RF passive

circuit and a smaller RF amplifier by enabling a three-dimensional location of a spiral inductor, a capacitor, and a via-hole. Moreover, a static capacity will be increased without increasing the occupancy, which will facilitate designing of such a circuit as a bias feeding circuit of an RF amplifier which inherently requires large capacity.

In addition, the RF amplifier of the present invention is characterized by utilizing the RF passive circuit equipped with a via-hole as a matching circuit, or as an RF choke of a bias feeding circuit.

Moreover, the RF passive circuit equipped with a via-hole is characterized by a metal film of the via-hole provided through a main surface of a semiconductor substrate which further extends along the main surface, and by a spiral metal layer formed on the extended part of the metal film, which works as an inductor with a dielectric layer in between. Here, the extended part of the metal film can be made in the same spiral pattern as the spiral inductor which is formed on the metal film.

The above structure enables to accommodate a static capacity where the extended part of the metal layer and the spiral metal layer face each other with a dielectric layer in between. This realizes a three-dimensional

location of a spiral inductor, a capacitor, and a via-hole, thereby reducing the occupancy thereof. This also helps to make a smaller RF passive circuit, and a smaller RF amplifier.

5 Moreover, the RF amplifier of the present invention is characterized by utilizing the RF passive circuit equipped with a via-hole as a matching circuit, or as an RF choke of a bias feeding circuit.

10 In addition, the RF passive circuit equipped with a via-hole that the present invention is applied to, is characterized by making a via-hole that goes through a semiconductor substrate, and by making a dielectric layer so as to cover a metal film of the via-hole which is provided through a main surface of the semiconductor substrate, and
15 by an inductor formed as a spiral metal layer which covers the dielectric layer so as to face against the metal film at one part, where a capacity element is held between the via-hole and the inductor.

20 The above structure enables a three dimensional location of a spiral inductor, a capacitor, and a via-hole from inside to the surface of the semiconductor substrate, thereby reducing the occupancy thereof, and helps to make a smaller RF passive circuit and a smaller RF amplifier.

 In addition, the RF amplifier of the present

invention is characterized by utilizing an RF passive circuit equipped with a via-hole as a matching circuit, or as an RF choke of a bias feeding circuit.

Moreover, the RF passive circuit with a via-hole that
5 the present invention is applied to, is characterized by being equipped with a via-hole that goes through a semiconductor substrate from the other main surface of the semiconductor substrate, and by having a dielectric layer on a metal film of a via-hole provided through the main
10 surface of a semiconductor substrate, and having a metal layer on the dielectric layer, and holding a capacity element between the metal film of the via-hole and the metal layer.

The above structure realizes a three dimensional
15 location of a capacitor and a via-hole on one semiconductor substrate, thereby reducing the occupancy thereof. This realizes a smaller RF passive circuit and a smaller RF amplifier.

In addition, the RF amplifier of the present
20 invention is characterized by electrically connecting a wiring metal layer of the RF passive circuit with a gate terminal of a common gate circuit of a FET, or with a base terminal of a common base circuit of a bipolar transistor, or by electrically connecting, with a source terminal of

a FET, a terminal which is a terminal of a resistance element electrically connected to the metal layer, so as to form a self bias circuit.

In addition, the RF passive circuit of the present invention equipped with a via-hole is characterized by making a via-hole that goes through a semiconductor substrate, and by forming a dielectric layer and a wiring metal layer on a metal film of the via-hole, in this order, so as to hold a capacity element between a ground metal layer and the wiring metal layer.

The above structure enables a three dimensional location of a capacitor and a via-hole on one semiconductor substrate, thereby reducing the occupancy thereof. This helps making a smaller RF passive circuit and a smaller RF amplifier.

Moreover, the RF amplifier of the present invention is characterized by electrically connecting a wiring metal layer of the RF passive circuit with a gate terminal of a common gate circuit of a FET, or by electrically connecting the wiring metal layer with a base terminal of a common base circuit in a bipolar transistor, or by connecting a terminal of a resistance element of the RF passive circuit with the ground metal layer, and the other terminal to the wiring metal layer, so as to form a self

bias circuit.

The RF passive circuit equipped with a via-hole that the present invention is applied to, is further characterized by making a via-hole that goes through a semiconductor substrate, and by forming, on a metal film of the via-hole, a first dielectric layer, a first wiring metal layer, a second dielectric layer, and a second wiring metal layer in this order. The RF passive circuit of the present invention is further characterized by having a first capacity element between the metal film and the first wiring metal layer, and the second capacity element between the first wiring metal layer and the second wiring metal layer, and by electrically connecting the metal film and the second wiring metal layer, so as to form a static capacity determined by a sum of the first capacity element and the second capacity element.

The RF amplifier of the present invention is further characterized by electrically connecting a first wiring metal layer of an RF passive circuit equipped with a via-hole with a gate terminal of a common gate circuit of a FET, or by electrically connecting a first wiring metal layer with a base terminal of a common base circuit of a bipolar transistor. Or the RF amplifier is characterized by electrically connecting one terminal of a resistance

element with the metal film, and the other terminal with the first wiring metal layer, and the terminal of the resistance element which is electrically connected with the second wiring metal layer is further electrically
5 connected with a source terminal of the FET so as to form a self bias circuit.

DESCRIPTION OF THE DRAWINGS

These and other objects, advantages and features of the invention will become apparent from the following description thereof taken in conjunction with the accompanying drawings which illustrate a specific embodiment of the invention. In the drawings:

Figs. 1A - 1D show an RF passive circuit and an RF amplifier equipped with via-holes according to the first embodiment of the present invention. Fig. 1A is a schematic circuit diagram that the RF passive circuit of the present invention is applied to. Fig. 1B is a plan view showing an electrode pattern constituting a matching circuit which
15 is one example of the RF passive circuit, and Fig. 1C is a plan view showing an electrode pattern constituting a bias feeding circuit which is another example of the RF passive circuit. Finally Fig. 1D is a cross-sectional view of Fig. 1B.

Figs. 2A - 2D show an RF passive circuit and an RF amplifier equipped with via-holes according to the second embodiment of the present invention. Fig. 2A is a schematic circuit diagram that the RF passive circuit of the present invention is applied to. Fig. 2B is a plan view showing an electrode pattern constituting a matching circuit which is one example of the RF passive circuit, and Fig. 2C is a plan view showing an electrode pattern constituting a bias feeding circuit which is another example of the RF passive circuit. Finally Fig. 2D is a cross-sectional view of Fig. 2B.

Figs. 3A - 3C show an RF passive circuit and an RF amplifier equipped with via-holes according to the third embodiment of the present invention. Fig. 3A is a schematic circuit diagram that the RF passive circuit is applied to. Fig. 3B is a plan view showing an electrode pattern constituting a matching circuit which is one example of the RF passive circuit, and Fig. 3C is a cross-sectional view of Fig. 3B.

Figs. 4A - 4D show an RF passive circuit and an RF amplifier equipped with via-holes according to the fourth embodiment of the present invention. Fig. 4A is a schematic circuit diagram that the RF passive circuit of the present invention is applied to. Fig. 4B is a plan view showing

an electrode pattern constituting a matching circuit which is one example of the RF passive circuit, and Fig. 4C is a plan view showing an electrode pattern constituting a bias feeding circuit which is another example of the RF passive circuit. Finally Fig. 4D is a cross-sectional view of Fig. 4B.

10 Figs. 5A - 5D show an RF passive circuit and an RF amplifier equipped with via-holes according to the fifth embodiment of the present invention. Figs. 5A - 5C are schematic circuit diagrams of the RF amplifier respectively. Fig. 5D is a cross-sectional view of a passive circuit formed on a GaAs substrate which is applied to each circuit in Figs. 5A - 5C.

15 Figs. 6A - 6C show an RF passive circuit and an RF amplifier equipped with via-holes according to the sixth embodiment of the present invention. Figs. 6A and 6B are schematic circuit diagrams of the RF amplifier, and Fig. 6C is a cross-sectional view of a passive circuit formed on a GaAs substrate which is applied to each circuit in 20 Figs. 6A and 6B.

Figs. 7A - 7C show an RF passive circuit and an RF amplifier equipped with via-holes according to the seventh embodiment of the present invention. Figs. 7A and 7B are schematic circuit diagrams of the RF amplifier, and Fig.

7C is a cross-sectional view of a passive circuit formed on a GaAs substrate which is applied to each circuit in Figs. 7A and 7B.

Figs. 8A - 8D show a conventional type of RF passive circuit and RF amplifier equipped with via-holes. Fig. 8A is a schematic diagram. Fig. 8B is a plan view showing a matching circuit formed on a substrate. Fig. 8C is a plan view showing a bias feeding circuit formed on a substrate, and Fig. 8D is a cross-sectional view of Fig. 8C.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The following is a description of RF passive circuits and RF amplifiers equipped with via-holes, which are the preferred embodiments of the present invention, with reference to the drawings.

1. First Embodiment

Figs. 1A - 1D are drawn to describe the first embodiment of the present invention.

Fig. 1A is a schematic circuit diagram of the RF amplifier and the RF passive circuit that the present invention is applied to. The circuit is basically the same as the one in Fig. 8A, with minor difference in reference numbers for parts and materials. Therefore description is

omitted.

Figs. 1B and 1C are both diagrams showing a plan view of structures realized by an input matching circuit portion 125 and a drain voltage feeding circuit 107 in Fig. 1 (1),
5 pertaining to the first embodiment.

Fig. 1B is a plan view of the input matching circuit portion 125. An input matching parallel inductor 114 is in a spiral-electrode-pattern, and an input matching parallel capacitor 115 is an MIM capacitor and is created
10 inside an input matching circuit via-hole 121, which is a surface via-hole made from the front surface of the GaAs substrate 124.

The following is a detailed description of the above-mentioned structure with reference to Fig. 1D, a cross-sectional diagram. The whole back surface of the GaAs
15 substrate 124 is covered by the back surface metal layer 127, and an insulator layer 134 is formed such as silicon oxide on an arbitrary part on the front surface of the GaAs substrate 124. On the front surface of the GaAs substrate
20 124 where the insulator layer 134 is not present, a via-hole 121 is formed by etching. On the insulator layer 134, a lower wiring metal layer 131 made by gold-plating is formed in a spiral pattern, which is covered by a between-layer insulator film 132 made of silicon nitride. This is then

covered by an upper wiring metal layer 130 made by gold/titanium plating. As Fig. 1B shows, the upper wiring metal layer 130 is in a linear form. The upper wiring metal layer 130 and the lower wiring metal layer 131 are connected to each other by a contact hole 133 going through the between-layer insulator film 132. Both metal layers, put together, constitute the input matching parallel inductor 114 equivalently.

The inside of the via-hole 121 is covered with a three-layer film made of: a ground metal layer 126, a dielectric layer 128, a first wiring metal layer for capacity element 129, from the bottom. The ground metal layer 126 contacts the back surface metal layer 127 on the bottom of the via-hole and it extends along the edge of the via-hole on the front surface of the GaAs substrate. The dielectric layer 128 is made of such material as titanium oxide strontium (SrTiO_3 : STO) whose permittivity is 100 or more. The first wiring metal layer for capacity element 129 extends on the between-layer insulator film 132 so as to merge with the upper wiring metal layer 130. The three-layer film forms the input matching parallel capacitor 115, which has a static capacity determined by the following elements: a permittivity of the dielectric layer 128, the space between the two metal layers 126 and

129, and the distance between the two layers.

The drain voltage feeding circuit 107 is structured basically the same as the input matching circuit depicted in Fig. 1B. The only difference is that a drain voltage terminal 136 is drawn from between a spiral inductor and a drain voltage feeding circuit via-hole 123 through a drawing wire 135. Further explanation is omitted accordingly.

The above structure, incorporating a capacitor into a via-hole, is more advantageous in making smaller terminals than conventional one that positions each element in different places.

Note that such devices as a bipolar transistor and a metal-oxide semiconductor field-effect transistor (MOSFET) are to be alternatively used as an active element of an RF amplifier.

Also note that although the description is confined to RF amplifiers, the present invention is applicable to other RF devices such as mixer, or VCO, too.

20

2. Second Embodiment

Figs. 2A - 2D are drawings depicted for the explanation of the second embodiment of the present invention. The application circuits will not be described

since they are the same as those of Fig. 1A. Fig. 2B depicts an input matching circuit, and Fig. 2C depicts a drain voltage feeding circuit. Fig. 2D is a cross-sectional view of both circuits.

5 The second embodiment has larger static capacity than the first embodiment, realized by an input matching parallel capacitor 221 created inside a via-hole 215. That is, the second embodiment has a five-layer film inside the via-hole 215 made by stacking: a ground metal layer 226,
10 a first dielectric layer 2281, a first wiring metal layer for capacity element 2291, a second dielectric layer 2282, and a second wiring metal layer for capacity element 2292, from the bottom. Note that the three metal layers are made of the same metal material, which is the same material
15 used in the first embodiment. Likewise, all the two dielectric layers, in this second embodiment, are made of the same dielectric material, which is the same material as the first embodiment. The five layers are connected in some parts; the first dielectric layer 2281 and the second
20 dielectric layer 2282 are connected at one end of both layers above the GaAs substrate, over which the ground metal layer 226 and the second wiring metal layer for capacity element 2292 are connected.

 This structure enables nearly twice as much space as

the first embodiment where the metal layers face each other, since both the ground metal layer 226 and the second wiring metal layer for capacity element 2292 are structured to face against the first wiring metal layer for capacity element 2291. Therefore, if the permittivity of the dielectric layer is the same, the static capacity will be nearly twice as large as the first embodiment. Moreover, it does not damage the advantage in making smaller terminals since the total occupancy stays the same as the first embodiment.

3. Third Embodiment

Figs. 3A - 3C are depicted for the explanation of the third embodiment.

Fig. 3A is a plan view showing a schematic circuit diagram for an RF amplifier the third embodiment is applied to. The circuits are the same as those depicted in Fig. 8A, whose description is omitted accordingly.

Fig. 3B shows a plan view of an input matching circuit portion 325 and a drain voltage feeding circuit 307, both as parts of an RF amplifier of the third embodiment. Fig. 3C is a cross-sectional view of Fig. 3B.

The following focuses on the input matching circuit portion 325 for detailed description.

First, a first wiring metal layer 330 is formed by gold/titanium vacuum evaporation in a spiral pattern seen from the above; it is formed so as to cover an insulator film 334 made of such materials as silicon oxide on a GaAs substrate 324. Next, a dielectric layer 328 made of titanium oxide strontium which has a permittivity of 100 or more is applied on the first wiring metal layer 330, in just about the same form as the first wiring metal layer 330, seen from the above. Then, the dielectric layer 328, in turn, is covered by a second wiring metal layer 331 made by gold-plating or gold/titanium vacuum evaporation, also in just about the same form as the rest. The center of the spiral of the first wiring metal layer 330 is connected, at the end, to a ground metal layer 326 above the via-hole, and is grounded by the ground metal layer 326 and the via-hole.

The third embodiment enables to have an input matching parallel capacitor 315 since the first wiring metal layer 330 is structured to face the second wiring metal layer 331 with the dielectric layer 328 in between. Moreover with this embodiment, the second wiring metal layer 331 is structured also to work as an inductor against high frequencies, as formed spirally and lengthy. Accordingly, the structure of Figs. 3B and 3C, by grounding

the capacitor at one end and connecting to an inductor at the other end, enables the input matching circuit portion 325 and the drain voltage feeding circuit 307 equivalently.

5 4. Fourth Embodiment

Figs. 4A - 4D are drawn to describe the fourth embodiment of the present invention.

Fig. 4A is a schematic circuit diagram for an RF passive circuit and an RF amplifier that this embodiment is applied to. The circuit in Fig. 4A is the same as Fig. 8A as self-explanatory, which does not probably need further explanation.

Figs. 4B and 4C are plan views showing an input matching circuit portion 425 and a drain voltage feeding circuit 407 respectively, both showing their circuit patterns, and Fig. 4D is a cross-sectional diagram thereof. The following description is confined to the input matching circuit portion, since it has many parts in common with the drain voltage feeding circuit 407.

20 An input matching circuit via-hole 421 is placed underneath the center of the spiral of an input matching parallel inductor 414.

The input matching circuit via-hole 421 is made using a backside via-hole method from the back of the GaAs

substrate 424. The ground metal layer 426, made by gold-plating or gold/titanium vacuum evaporation, is on the via-hole 421 and is conducted to the backside ground metal layer 427.

5 On the ground metal layer 426, a dielectric layer 428 made of titanium oxide strontium (SrTiO₃:STO) with a permittivity of 100 or more is formed, which has approximately the same form as the ground metal layer 426 seen from the above. On this dielectric layer 428, in turn,
10 a lower wiring metal 429 is formed by gold/titanium vacuum evaporation. An MIM capacitor formed by the ground metal layer 426, the dielectric layer 428, and the lower wiring metal 429 put together, makes an input matching parallel capacitor 415.

15 Around the MIM capacitor and on the GaAs substrate 424, a between-layer insulator film 432 and an insulator film 434 made of silicon oxide for example are formed, which are then covered by an upper wire 430 in a spiral pattern made by such method as gold/titanium vacuum evaporation
20 method. The center of the upper wire 430 is conducted to the lower wiring metal 429 via a contact hole 433. The upper wire 430 and the lower wiring metal 429 form a spiral-formed inductor.

The fourth embodiment, just as the third embodiment,

grounds one end of the capacitor, while connecting the other end to the inductor, which forms equivalently the input matching circuit portion 425 depicted in Fig. 4A.

5 5. Fifth Embodiment

Figs. 5A - 5D are drawn to describe the fifth embodiment of the present invention.

Fig. 5A shows a schematic circuit diagram of an RF amplifier that the fifth embodiment is applied to.

10 The RF amplifier depicted in Fig. 5A uses a common gate type FET. A bypass capacitor 536 and a gate voltage terminal 537 are connected to a gate terminal 502 of a FET 501; the bypass capacitor 536 is grounded by a ground via-hole 539. An input matching circuit 506 and a choke inductor 540 are connected to a source terminal 504, and at the terminal of the choke inductor 540, a source voltage terminal 538 is connected. A drain terminal 503 is connected to an output matching circuit 508, a choke inductor 519, and a bypass capacitor 520. An input terminal 15 510 and an output terminal 511 are both 50Ω impedance, and the input matching circuit 506 and the output matching circuit 508 are adjusted to 50Ω .

The structures described in the first, second, third, and fourth embodiments, are applicable to the input

matching circuit 506 and the output matching circuit 508.

Fig. 5B is a schematic circuit diagram showing an RF amplifier using a common base type bipolar transistor. A bypass capacitor 536 and a base voltage terminal 543 are connected to a base terminal 542 of a bipolar transistor 541. The bypass capacitor 536 is grounded by the ground via-hole 539. An input matching circuit 506 and a choke inductor 540 are connected to an emitter terminal 544. At the terminal of the choke inductor 540, an emitter voltage terminal 545 is connected. Finally an output matching circuit 508, a choke inductor 519, and a bypass capacitor 520 are connected to a collector terminal 546. Both of an input terminal 510 and an output terminal 511 are 50Ω impedance, and both of the input matching circuit 506 and the output matching terminal 508 are adjusted to 50Ω .

The structures described in the first, second, third, and fourth embodiments are applicable to the input matching circuit 506 and the output matching circuit 508.

Fig. 5C is a schematic circuit diagram showing an RF amplifier using a source ground type FET which uses a self-bias method. A gate bias resistance 505 and an input matching circuit 506 are connected to a gate terminal 502 of a FET 501. A self bias resistance 547 and a self bias bypass capacitor 548 are connected to a source terminal

504, which is grounded by a ground via-hole 538. Finally an output matching circuit 508 a choke inductor 519, and a bypass capacitor 520 are connected to a drain terminal 503. An input terminal 510 and an output terminal 511 are
5 both 50Ω impedance, and the input matching circuit 506 and the output matching circuit 508 are adjusted to 50Ω .

The structures described in the first, second, third, and fourth embodiment are applicable to the input matching circuit 506 and the output matching circuit 508.

FIG. 5D

10 Fig. 5D is a cross-sectional view of a circuit pattern constituting a capacitor grounded by a via-hole at one end.

The ground via-hole 539 depicted in Figs. 5A - 5C is made by a backside via-hole method from the back of the GaAs substrate 524. The ground metal layer 526, made by
15 gold-plating or gold/titanium vacuum evaporation, is conducted to the backside ground metal layer 527 of the GaAs substrate 524.

A dielectric layer 528 which is made of titanium oxide strontium ($\text{SrTiO}_3\text{:STO}$) with a permittivity of 100 or more
20 is formed on the ground metal layer 526. On this dielectric layer 528, a wiring metal 529 is formed by such method as gold/titanium vacuum evaporation. A bypass capacitor 536 and a self bias bypass capacitor 548 are formed using a MIM capacitor, which is obtained by combining the ground

metal layer 526, the dielectric layer 528, and the wiring metal 529.

The circuit structure depicted in Figs. 5A and 5B is obtained by electrically connecting the wiring metal 529
5 and the gate terminal 502.

Furthermore, the circuit structure in Fig. 5C is obtained by electrically connecting one end of the self bias resistance 547 to the wiring metal 529, and the other
10 end to the ground metal layer 526. Or, the circuit structure is alternatively obtained by using the insulator layer 534 formed around the dielectric layer 528 as a resistance layer, substituting it for the self bias resistance 547.

The fifth embodiment is structured to enable to make smaller terminals by placing the via-hole and the capacitor
15 in the same position on the substrate.

6. Sixth Embodiment

Figs. 6A - 6C are drawn to explain the sixth embodiment.

Fig. 6A shows an RF amplifier that the sixth
20 embodiment is applied to.

Figs. 6A and 6B are the same as Figs. 5A and 5B respectively. Explanation of the circuit pertaining Fig. 6A and 6B is omitted accordingly.

The circuit described in the first, second, third,

and fourth embodiments of the present invention (i.e. Figs. 1A, 2A, 3A, and 4A) is applicable to an input matching circuit 606 and an output matching circuit 608.

5 A ground via-hole 638 depicted in Figs. 6A - 6C is formed by a surface via-hole method from the front surface of a GaAs substrate 624. Inside the ground via-hole 638, a bypass capacitor 636 and a self bias bypass capacitor 648 are formed. A ground metal layer 626 is formed, by gold-plating or gold/titanium vacuum evaporation, both
10 inside and around the via-hole on the GaAs substrate 624. The ground metal layer 626 is conducted to a backside ground metal layer 627 on the GaAs substrate 624. A dielectric layer 628 made of titanium oxide strontium (SrTiO₃:STO) which has a permittivity of 100 or more is formed on the
15 ground metal layer 626. On the dielectric layer 628, in turn, a first wiring metal layer for capacity element 629 is formed by such method as a gold/titanium vacuum evaporation method. From the above, a bypass capacitor 636 and a self bias bypass capacitor 648 are formed as capacitor
20 elements, by the ground metal layer 626, the first wiring metal layer for capacity element 629, and the dielectric layer 628.

7. Seventh Embodiment

Figs. 7A - 7C show the seventh embodiment of the present invention, which has a larger capacitor than the sixth embodiment.

5 The seventh embodiment is mostly the same as the sixth embodiment except how the capacitor is structured. The following description focuses on this point accordingly.

10 As Fig. 7C shows, a ground via-hole 738 is made from the front surface of a GaAs substrate 724 using a surface via-hole method, so as to form a bypass capacitor inside. A ground metal layer 726 is made inside the ground via-hole 738 and also around the upper part thereof by gold-plating or gold/titanium vacuum evaporation. The ground metal layer is conducted to a backside ground metal layer 727.

15 On the ground metal layer 726, a first dielectric layer 7281 is formed which is made of titanium oxide strontium (SrTiO₃:STO) with a permittivity of 100 or more. Then, on this first dielectric layer 7281, a first wiring metal layer for capacity element 7291 is made by such method as

20 gold/titanium vacuum evaporation.

Further, on the first wiring metal layer for capacity element 7291, a second dielectric layer 7282 is formed made of titanium oxide strontium (SrTiO₃:STO) with a permittivity of 100 or more, which is in turn covered by

a second wiring metal layer for capacity element 7292 made by such method as gold/titanium vacuum evaporation. Note that the ground metal layer 726 and the second wiring metal layer for capacity element 7292 are electrically
5 connected.

The seventh embodiment is thus structured to create two capacity elements; the first capacity element by means of the ground metal layer 726, the first wiring metal layer for capacity element 7291, and the first dielectric layer
10 7281; and the second capacity element by means of the first wiring metal layer for capacity element 7291, the second wiring metal layer for capacity element 7292, and the second dielectric layer 7282. From equivalent circuit point of view, a bypass capacitor is created by connecting
15 the first capacity element and the second capacity element in parallel (i.e. the capacity being a sum of the first and the second capacity elements).

Although the present invention has been fully described by way of examples with reference to the
20 accompanying drawings, it is to be noted that various changes and modifications will be apparent to those skilled in the art.

Therefore, unless such changes and modifications depart from the scope of the present invention, they should

be construed as being included therein.

0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
94
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122
123
124
125
126
127
128
129
130
131
132
133
134
135
136
137
138
139
140
141
142
143
144
145
146
147
148
149
150
151
152
153
154
155
156
157
158
159
160
161
162
163
164
165
166
167
168
169
170
171
172
173
174
175
176
177
178
179
180
181
182
183
184
185
186
187
188
189
190
191
192
193
194
195
196
197
198
199
200
201
202
203
204
205
206
207
208
209
210
211
212
213
214
215
216
217
218
219
220
221
222
223
224
225
226
227
228
229
230
231
232
233
234
235
236
237
238
239
240
241
242
243
244
245
246
247
248
249
250
251
252
253
254
255
256
257
258
259
260
261
262
263
264
265
266
267
268
269
270
271
272
273
274
275
276
277
278
279
280
281
282
283
284
285
286
287
288
289
290
291
292
293
294
295
296
297
298
299
300
301
302
303
304
305
306
307
308
309
310
311
312
313
314
315
316
317
318
319
320
321
322
323
324
325
326
327
328
329
330
331
332
333
334
335
336
337
338
339
340
341
342
343
344
345
346
347
348
349
350
351
352
353
354
355
356
357
358
359
360
361
362
363
364
365
366
367
368
369
370
371
372
373
374
375
376
377
378
379
380
381
382
383
384
385
386
387
388
389
390
391
392
393
394
395
396
397
398
399
400
401
402
403
404
405
406
407
408
409
410
411
412
413
414
415
416
417
418
419
420
421
422
423
424
425
426
427
428
429
430
431
432
433
434
435
436
437
438
439
440
441
442
443
444
445
446
447
448
449
450
451
452
453
454
455
456
457
458
459
460
461
462
463
464
465
466
467
468
469
470
471
472
473
474
475
476
477
478
479
480
481
482
483
484
485
486
487
488
489
490
491
492
493
494
495
496
497
498
499
500
501
502
503
504
505
506
507
508
509
510
511
512
513
514
515
516
517
518
519
520
521
522
523
524
525
526
527
528
529
530
531
532
533
534
535
536
537
538
539
540
541
542
543
544
545
546
547
548
549
550
551
552
553
554
555
556
557
558
559
560
561
562
563
564
565
566
567
568
569
570
571
572
573
574
575
576
577
578
579
580
581
582
583
584
585
586
587
588
589
590
591
592
593
594
595
596
597
598
599
600
601
602
603
604
605
606
607
608
609
610
611
612
613
614
615
616
617
618
619
620
621
622
623
624
625
626
627
628
629
630
631
632
633
634
635
636
637
638
639
640
641
642
643
644
645
646
647
648
649
650
651
652
653
654
655
656
657
658
659
660
661
662
663
664
665
666
667
668
669
670
671
672
673
674
675
676
677
678
679
680
681
682
683
684
685
686
687
688
689
690
691
692
693
694
695
696
697
698
699
700
701
702
703
704
705
706
707
708
709
710
711
712
713
714
715
716
717
718
719
720
721
722
723
724
725
726
727
728
729
730
731
732
733
734
735
736
737
738
739
740
741
742
743
744
745
746
747
748
749
750
751
752
753
754
755
756
757
758
759
760
761
762
763
764
765
766
767
768
769
770
771
772
773
774
775
776
777
778
779
780
781
782
783
784
785
786
787
788
789
790
791
792
793
794
795
796
797
798
799
800
801
802
803
804
805
806
807
808
809
810
811
812
813
814
815
816
817
818
819
820
821
822
823
824
825
826
827
828
829
830
831
832
833
834
835
836
837
838
839
840
841
842
843
844
845
846
847
848
849
850
851
852
853
854
855
856
857
858
859
860
861
862
863
864
865
866
867
868
869
870
871
872
873
874
875
876
877
878
879
880
881
882
883
884
885
886
887
888
889
890
891
892
893
894
895
896
897
898
899
900
901
902
903
904
905
906
907
908
909
910
911
912
913
914
915
916
917
918
919
920
921
922
923
924
925
926
927
928
929
930
931
932
933
934
935
936
937
938
939
940
941
942
943
944
945
946
947
948
949
950
951
952
953
954
955
956
957
958
959
960
961
962
963
964
965
966
967
968
969
970
971
972
973
974
975
976
977
978
979
980
981
982
983
984
985
986
987
988
989
990
991
992
993
994
995
996
997
998
999
1000
1001
1002
1003
1004
1005
1006
1007
1008
1009
1010
1011
1012
1013
1014
1015
1016
1017
1018
1019
1020
1021
1022
1023
1024
1025
1026
1027
1028
1029
1030
1031
1032
1033
1034
1035
1036
1037
1038
1039
1040
1041
1042
1043
1044
1045
1046
1047
1048
1049
1050
1051
1052
1053
1054
1055
1056
1057
1058
1059
1060
1061
1062
1063
1064
1065
1066
1067
1068
1069
1070
1071
1072
1073
1074
1075
1076
1077
1078
1079
1080
1081
1082
1083
1084
1085
1086
1087
1088
1089
1090
1091
1092
1093
1094
1095
1096
1097
1098
1099
1100
1101
1102
1103
1104
1105
1106
1107
1108
1109
1110
1111
1112
1113
1114
1115
1116
1117
1118
1119
1120
1121
1122
1123
1124
1125
1126
1127
1128
1129
1130
1131
1132
1133
1134
1135
1136
1137
1138
1139
1140
1141
1142
1143
1144
1145
1146
1147
1148
1149
1150
1151
1152
1153
1154
1155
1156
1157
1158
1159
1160
1161
1162
1163
1164
1165
1166
1167
1168
1169
1170
1171
1172
1173
1174
1175
1176
1177
1178
1179
1180
1181
1182
1183
1184
1185
1186
1187
1188
1189
1190
1191
1192
1193
1194
1195
1196
1197
1198
1199
1200
1201
1202
1203
1204
1205
1206
1207
1208
1209
1210
1211
1212
1213
1214
1215
1216
1217
1218
1219
1220
1221
1222
1223
1224
1225
1226
1227
1228
1229
1230
1231
1232
1233
1234
1235
1236
1237
1238
1239
1240
1241
1242
1243
1244
1245
1246
1247
1248
1249
1250
1251
1252
1253
1254
1255
1256
1257
1258
1259
1260
1261
1262
1263
1264
1265
1266
1267
1268
1269
1270
1271
1272
1273
1274
1275
1276
1277
1278
1279
1280
1281
1282
1283
1284
1285
1286
1287
1288
1289
1290
1291
1292
1293
1294
1295
1296
1297
1298
1299
1300
1301
1302
1303
1304
1305
1306
1307
1308
1309
1310
1311
1312
1313
1314
1315
1316
1317
1318
1319
1320
1321
1322
1323
1324
1325
1326
1327
1328
1329
1330
1331
1332
1333
1334
1335
1336
1337
1338
1339
1340
1341
1342
1343
1344
1345
1346
1347
1348
1349
1350
1351
1352
1353
1354
1355
1356
1357
1358
1359
1360
1361
1362
1363
1364
1365
1366
1367
1368
1369
1370
1371
1372
1373
1374
1375
1376
1377
1378
1379
1380
1381
1382
1383
1384
1385
1386
1387
1388
1389
1390
1391
1392
1393
1394
1395
1396
1397
1398
1399
1400
1401
1402
1403
1404
1405
1406
1407
1408
1409
1410
1411
1412
1413
1414
1415
1416
1417
1418
1419
1420
1421
1422
1423
1424
1425
1426
1427
1428
1429
1430
1431
1432
1433
1434
1435
1436
1437
1438
1439
1440
1441
1442
1443
1444
1445
1446
1447
1448
1449
1450
1451
1452
1453
1454
1455
1456
1457
1458
1459
1460
1461
1462
1463
1464
1465
1466
1467
1468
1469
1470
1471
1472
1473
1474
1475
1476
1477
1478
1479
1480
1481
1482
1483
1484
1485
1486
1487
1488
1489
1490
1491
1492
1493
1494
1495
1496
1497
1498
1499
1500
1501
1502
1503
1504
1505
1506
1507
1508
1509
1510
1511
1512
1513
1514
1515
1516
1517
1518
1519
1520
1521
1522
1523
1524
1525
1526
1527
1528
1529
1530
1531
1532
1533
1534
1535
1536
1537
1538
1539
1540
1541
1542
1543
1544
1545
1546
1547
1548
1549
1550
1551
1552
1553
1554
1555
1556
1557
1558
1559
1560
1561
1562
1563
1564
1565
1566
1567
1568
1569
1570
1571
1572
1573
1574
1575
1576
1577
1578
1579
1580
1581
1582
1583
1584
1585
1586
1587
1588
1589
1590
1591
1592
1593
1594
1595
1596
1597
1598
1599
1600
1601
1602
1603
1604
1605
1606
1607
1608
1609
1610
1611
1612
1613
1614
1615
1616
1617
1618
1619
1620
1621
1622
1623
1624
1625
1626
1627
1628
1629
1630
1631
1632
1633
1634
1635
1636
1637
1638
1639
1640
1641
1642
1643
1644
1645
1646
1647
1648
1649
1650
1651
1652
1653
1654
1655
1656
1657
1658
1659
1660
1661
1662
1663
1664
1665
1666
1667
1668
1669
1670
1671
1672
1673
1674
1675
1676
1677
1678
1679
1680
1681
1682
1683
1684
1685
1686
1687
1688
1689
1690
1691
1692
1693
1694
1695
1696
1697
1698
1699
1700
1701
1702
1703
1704
1705
1706
1707
1708
1709
1710
1711
1712
1713
1714
1715
1716
1717
1718
1719
1720
1721
1722
1723
1724
1725
1726
1727
1728
1729
1730
1731
1732
1733
1734
1735
1736
1737
1738
1739
1740
1741
1742
1743
1744
1745
1746
1747
1748
1749
1750
1751
1752
1753
1754
1755
1756
1757
1758
1759
1760
1761
1762
1763
1764
1765
1766
1767
1768
1769
1770
1771
1772
1773
1774
1775
1776
1777
1778
1779
1780
1781
1782
1783
1784
1785
1786
1787
1788
1789
1790
1791
1792
1793
1794
1795
1796
1797
1798
1799
1800
1801
1802
1803
1804
1805
1806
1807
1808
1809
1810
1811
1812
1813
1814
1815
1816
1817
1818
1819
1820
1821
1822
1823
1824
1825
1826
1827
1828
1829
1830
1831
1832
1833
1834
1835
1836
1837
1838
1839
1840
1841
1842
1843
1844
1845
1846
1847
1848
1849
1850
1851
1852
1853
1854
1855
1856
1857
1858
1859
1860
1861
1862
1863
1864
1865
1866
1867
1868
1869
1870
1871
1872
1873
1874
1875
1876
1877
1878
1879
1880
1881
1882
1883
1884
1885
1886
1887
1888
1889
1890
1891
1892
1893
1894
1895
1896
1897
1898
1899
1900
1901
1902
1903
1904
1905
1906
1907
1908
1909
1910
1911
1912
1913
1914
1915
1916
1917
1918
1919
1920
1921
1922
1923
1924
1925
1926
1927
1928
1929
1930
1931
1932
1933
1934
1935
1936
1937
1938
1939
1940
1941
1942
1943
1944
1945
1946
1947
1948
1949
1950
1951
1952
1953
1954
1955
1956
1957
1958
1959
1960
1961
1962
1963
1964
1965
1966
1967
1968
1969
1970
1971
1972
1973
1974
1975
1976
1977
1978
1979
1980
1981
1982
1983
1984
1985
1986
1987
1988
1989
1990
1991
1992
1993
1994
1995
1996
1997
1998
1999
2000
2001
2002
2003
2004
2005
2006
2007
2008
2009
2010
2011
2012
2013
2014
2015
2016
2017
2018
2019
2020
2021
2022
2023
2024
2025
2026
2027
2028
2029
2030
2031
2032
2033
2034
2035
2036
2037
2038
2039
2040
2041
2042
2043
2044
2045
2046
2047
2048
2049
2050
2051
2052
2053
2054
2055
2056
2057
2058
2059
2060
2061
2062
2063
2064
2065
2066
2067
2068
2069
2070
2071
2072
2073
2074
2075
2076
2077
2078
2079
2080
2081
2082
2083
2084
2085
2086
2087
2088
2089
2090
2091
2092
2093
2094
2095
2096
2097
2098
2099
2100
2101
2102
2103
2104
2105
2106
2107
2108
2109
2110
2111
2112
2113
2114
2115
2116
2117
2118
2119
2120
2121
2122
2123
2124
2125
2126
2127
2128
2129
2130
2131
2132
2133
2134
2135
2136
2137
2138
2139
2140
2141
2142
2143
2144
2145
2146
2147
2148
2149
2150
2151
2152
2153
2154
2155
2156
2157
2158
2159
2160
2161
2162
2163
2164
2165
2166
2167
2168
2169
2170
2171
2172
2173
2174
2175
2176
2177
2178
2179
2180
2181
2182
2183
2184
2185
2186
2187
2188
2189
2190
2191
2192
2193
2194
2195
2196
2197
2198
2199
2200
2201
2202
2203
2204
2205
2206
2207
2208
2209
2210
2211
2212
2213
2214
2215
2216
2217
2218
2219
2220
2221
2222
2223
2224
2225
2226
2227
2228
2229
2230
2231
2232
2233
2234
2235
2236
2237